IMPLEMENTATION OF MCP-BASED WIMAX RECEIVER TEST-BED FOR RECONFIGURABLE MOBILE DEVICE CONSIDERING ETSI RRS STANDARD

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ABSTRACT

This paper presents an implementation of MCP (Mobile Computing Platform)-based reconfigurable MD (Mobile Device), of which the main objective is to verify the feasibility and performance of reconfigurable MD that is being standardized in ETSI (European Telecommunications Standards Institute) RRS (Reconfigurable Radio Systems). SDR (Software Defined Radio) platform in general requires a lot of arithmetic signal processing procedures, which brings about several restrictions in implementing the SDR platform using conventional MCP because conventional MCP consists of mobile processor only. In order to resolve those restrictions, we have adopted OMAP (Open Multimedia Application Platform) as a software modem platform, which itself is a mobile processor consisting of ARM (Advanced RISC Machine) and DSP (Digital Signal Processor) that are capable of high-speed digital signal processing. We propose an MCP-based SDR platform architecture that fully supports on-going ETSI RRS standard using OMAP and FPGAs (Field Programmable Gate Array). In order to verify the proposed architecture, WiMAX (Worldwide interoperability for Microwave Access) waveform has been selected for the proposed receiver test-bed. Performance of the implemented test-bed is shown in terms of software modem run-time, which guarantees that the baseband signal processing in accordance with the ETSI RRS standard can fully be supported by the proposed MCP-based platform test-bed in real-time.

1. INTRODUCTION

Reconfigurable MD (Mobile Device) standard is being developed in ETSI (European Telecommunications Standards Institute) RRS (Reconfigurable Radio Systems) in such a way that RA (Radio Application) codes can be download from an on-line application store for various mobile communication standards [1]-[3].

According to the concept of the ETSI RRS standardization, RA codes that are provided by 3rd party will be available in on-line market, namely, Radio AppStore [4]. Figure 1 illustrates the concept of reconfigurable MD discussed in ETSI RRS.

Figure 1. Concept of ETSI RRS reconfigurable MD [4]

In order to realize the reconfigurable MD which is compliant with the ETSI RRS standard, it is necessary to standardize some BBIs (BaseBand Interfaces) needed for implementation of core function blocks of RA codes to be supported in MD. Using the standardized BBIs, RA codes can be generated independently of modem chip, which means RA codes of various communication standards can be supported on a single platform. In this paper, we have implemented a test-bed MD platform using OMAP (Open Multimedia Application Platform) for verification of BBIs

to be standardized by ETSI RRS. For our implementation, WiMAX (Worldwide interoperability for Microwave Access) as an example of desired RA.

This paper is organized as follows. Section 2 introduces the entire architecture of WiMAX receiver implemented using OMAP and FPGA (Field Programmable Gate Array). Section 3 explains the implementation of WiMAX receiver. Section 4 provides a profiling result of RF (Radio Frequency) tests and digital signal processing block of the implemented WiMAX receiver. Finally, Section 5 concludes the implementation results.

2. SYSTEM ARCHITECTURE

Figure 2 illustrates the architecture of MCP (Mobile Computing Platform)-based reconfigurable MD platform. As shown in the figure, it consists of OMAP (OMAP3530), FPGA (Virtex-5 XC5VSX35T), and RF board (RFX2400). OMAP consists of DSP (Digital Signal Processor) and ARM (Advanced RISC Machine) which are for signal processing and control of the RA signals, respectively, while the FPGA board handles RF-related processing such as ADC/DDC (Analog to Digital Converter/Digital Down Converter), receive signal buffering, etc and relatively complicated procedures such as Viterbi decoding. Note that the implemented system performs the downlink only, i.e., receive only, because the objective is to verify the configuration capability of MD platform through the download of RA codes from the Radio AppStore [4] in accordance with the ETSI RRS standardization [1]-[3].

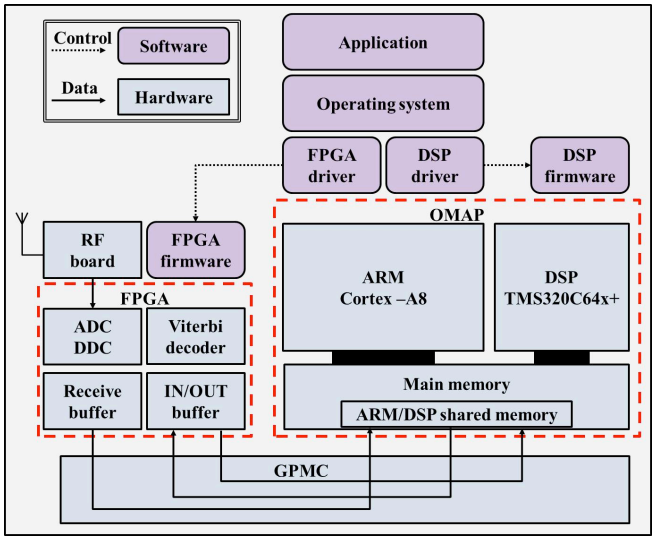


Figure 2. Architecture of MCP-based reconfigurable MD platform for WiMAX application

RF signal received through the antenna, as shown in Figure 2, is first frequency-down converted on RF board. Then, it is processed by ADC and DDC on FPGA board to be stored in the receive buffer. ARM processor shown in Figure 2 is operating on Android OS (Operating System) to control the interrupt of DSP and FPGA.

DSP driver and FPGA driver provide API (Application Programming Interface) for controlling each firmware on Android OS [5]. DSP firmware controls the DSP for the digital signal processing such as frame synchronization, FFT (Fast Fourier Transform), channel estimation, etc, while FPGA firmware controls the FPGA for the other part of signal processing such as Viterbi decoding, ADC, and DDC.

OMAP3530 processor adopted in our implementation is a typical MCP equipped with an ARM Cortex-A8 core, which is capable of 600MHz to 1GHz of processing speed with less than 300mW power consumption. Especially, its architecture of SIMD (Single Instruction Multiple Data) is capable of handling maximum four 32-bit data simultaneously [6].

In addition to the ARM Cortex-A8 core, OMAP 3530 includes a DSP, TMS320C64x+, as a co-processor. The DSP included in our implemented platform, TMS320C64x+, is equipped with 6 ALUs (Arithmetic and Logic Unit), sixty four 32-bit registers, and capable of processing eight 32-bit instructions per cycle with 430MHz operation speed [7].

FPGA adopted in our implemented system is Virtex-5 XC5VSX35T consists of 5,440 CLBs (Configurable Logic Blocks), 360 I/O (Input/Output), 3,024kb block memory, and 192 DSP48E slices, for high-speed digital signal processing [8].

3. WIMAX RECIVER IMPLEMENTATION

3.1 RF board and FPGA board

Figure 3 illustrates how the RF signals received at RF board and FPGA board are converted into baseband signals. Signal captured at antenna is down-converted through AMP (Amplifier) and modulator mixer as shown in Figure 3. Down-converted signal is converted into corresponding 2x14bit complex-valued digital data of 64MSamples/s via ADC and DDC procedure.

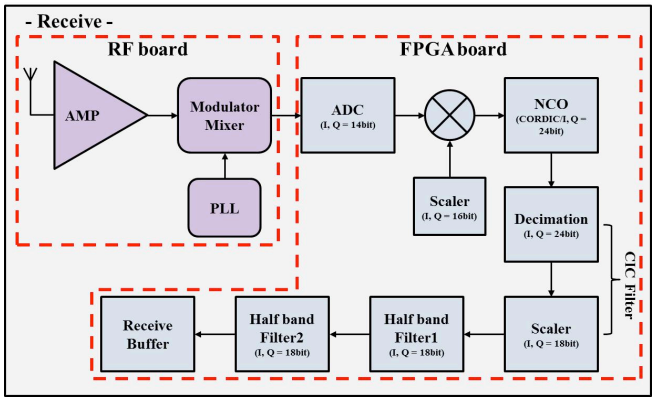


Figure 3. Block diagram of RF and FPGA board

Down conversion to baseband signal is possible just to use PLL (Phase Locked Loop) and Modulator Mixer in RF board. However, any frequency band is set to receive if PLL step size for the locking due to the presence of all frequencies can be adjusted. In the test-bed that is implemented in this paper, down conversion block process is performed to complement this functional limitation in FPGA.

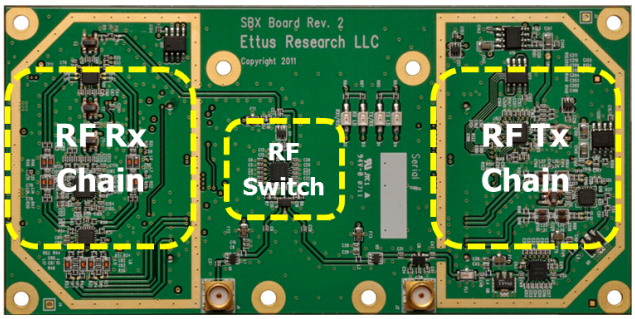


Figure 4. RFX2400 RF board

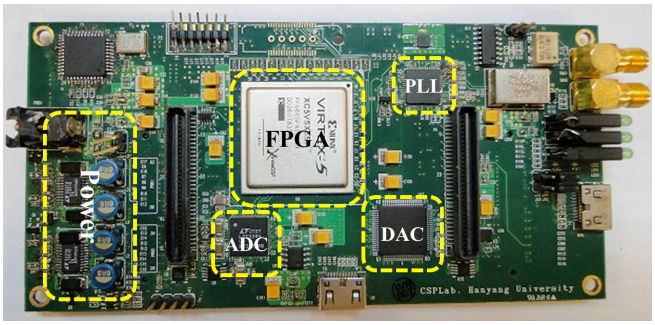


Figure 5. FPGA board

Figure 4 and 5 illustrate RF board and FPGA board implemented in our system, respectively. In RF board, as shown in Figure 4, Rx (Receiver) chain and Tx (Transmitter) chain for receive and transmit of signals, respectively, and RF switch for switching Rx and Tx is equipped, although the Tx chain is not used in our experimental test as mentioned earlier.

FPGA board shown in Figure 5 includes not only FPGA but also PLL, ADC/DAC, power, which are for storing receive signals after converting RF signal into baseband.

3.2 Baseband signal processing using DSP and FPGA

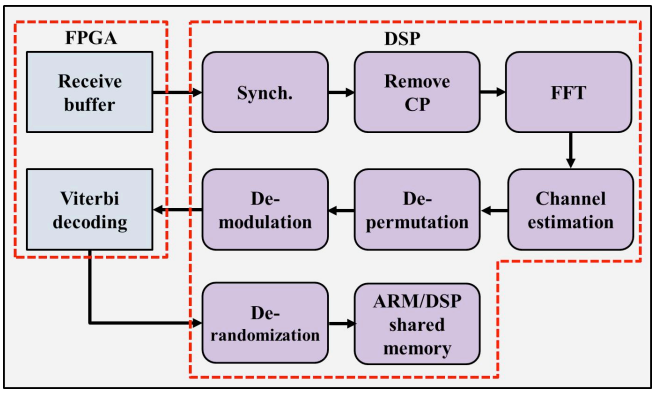


Figure 6. Block diagram of WiMAX radio application

Figure 6 illustrates a block diagram of software modem of the implemented WiMAX receiver. First, the received data stored at the receive buffer are brought into ARM/DSP shared memory through GPMC (General purpose Memory Controller). Then, DSP acquires frame synchronization from the data stored at ARM/DSP shared memory, removes CP (Cyclic Prefix), and performs the receiving procedures of WiMAX data, i.e., FFT, channel estimation, de-permutation, de-modulation [9].

Demodulated data are brought back to FPGA through GPMC to be processed with Viterbi decoder, which requires the most complicated operations among all the digital signal processing procedures [10]. Data processed at the Viterbi decoder are then stored at the ARM/DSP shared memory to retrieve the transmitted information through the de-randomization procedure.

4. EXPERIMENTAL RESULTS

The implemented MD system is of a layered structure with three layers consisting of RF board, FPGA board, and OMAP board as shown in Figure 7. On OMAP board, LCD (Liquid Crystal Display) is equipped to check the processing status during decoding or replaying video data. In addition, OMAP includes WiFi module as well as ARM and DSP, for downloading the RA codes from the Radio AppStore as

mentioned earlier. It particularly means that the RA code for WiMAX is downloaded through WiFi waveform from the Radio AppStore to our implemented MD system. The procedure of downloading the RA codes is not included in this paper, however.

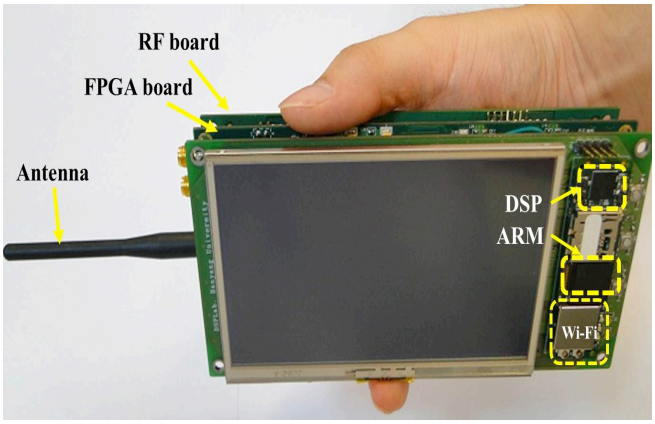


Figure 7. Implemented WiMAX receiver test-bed

4.1 RF test

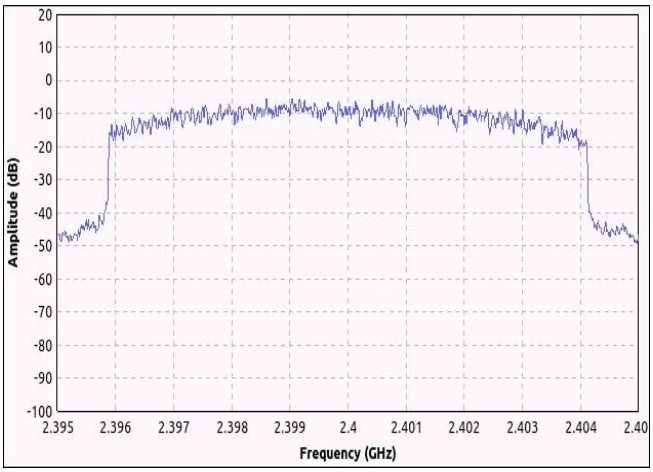


Figure 8. Spectrum of WiMAX signal

Figure 8 illustrates the spectrum of WiMAX signal measured after the signal passes through the RF and FPGA board. Transmit signal is WiMAX signal centered at 2.4 GHz with 10MHz bandwidth. As shown in Figure 8, it can be observed that received signal is located at the very center frequency, i.e., 2.4GHz with bandwidth of 10MHz.

4.2 Profiling

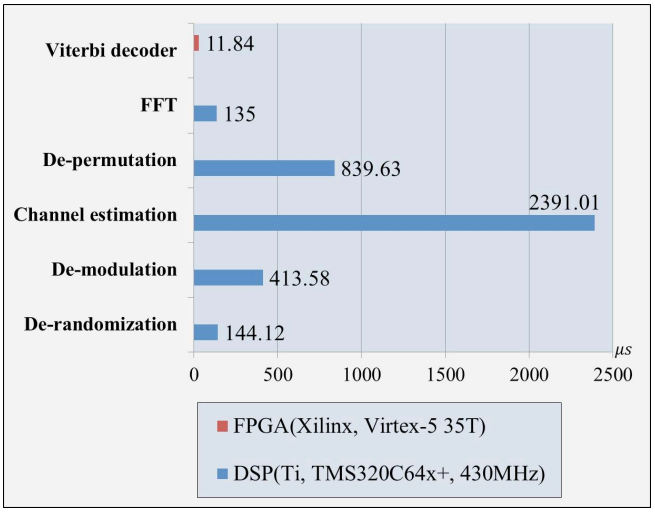
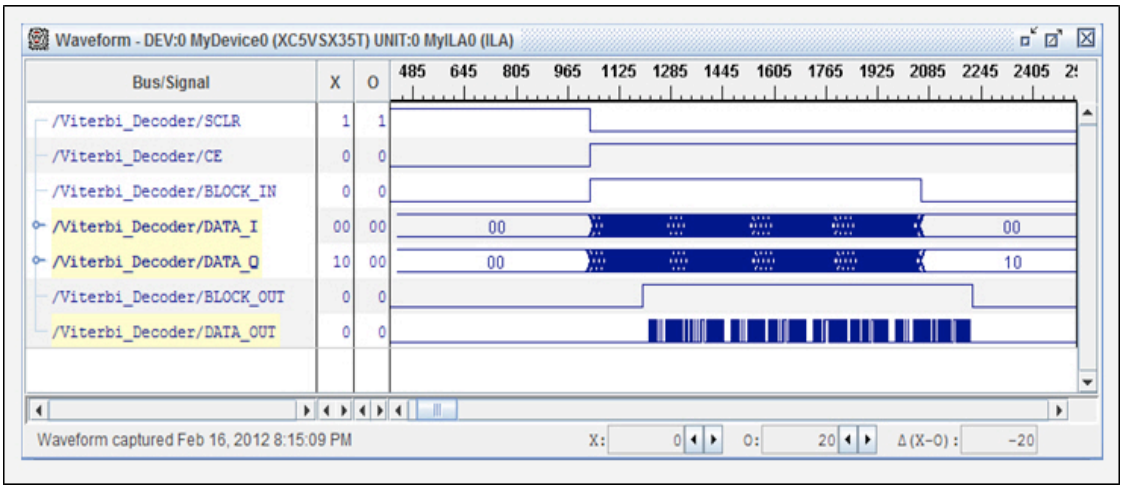


Table 1. WiMAX receiver processing time

Table 1 shows a profile of processing time for each operation required in the implemented WiMAX receiver MD measured at DSP and FPGA. As mentioned earlier, FFT, de-permutation, channel estimation, demodulation, and de-randomization are performed at DSP while FPGA takes care of all the other operations such as ADC/DDC and Viterbi decoder. Profiling the procedures of decoding the received signal, total computation time required for digital signal processing of each data frame is about 3.94ms, which is a lot shorter than 5ms frame period of WiMAX system. Consequently, our implemented MD system is capable of processing the WiMAX data in real-time.

4.3 Viterbi decoder test

In order to verify the Viterbi decoder implemented in Verilog HDL (Hardware Description Language), ChipScope Pro, an analyzing tool for real-time FPGA operation, has been utilized in our experimental tests. Viterbi decoder implemented in our system adopts 1/2 coding rate and is capable of decoding 3.46Mbps. As shown in Figure 9, Viterbi decoding is performed normally while, verified in Table 1 of section 4.2, the processing time for Viterbi decoding of 34,560 bits in each frame is only about 11.84us.



5. CONCLUSION

We implemented a test-bed platform of a reconfigurable MD for verifying the feasibility and real-time capability of the reconfigurable MD, for which function blocks for its software modem code are being standardized in ETSI RRS. The test-bed platform implemented in this paper consists of three layers, i.e., RF board, FPGA board, and OMAP board. FPGA and DSP in OMAP perform all the baseband signal processing required in WiMAX which has been chosen as an example waveform for the verification in this work. Meanwhile, ARM core in OMAP adopts Android OS to control the FPGA and DSP. Though we have arbitrarily selected WiMAX as an example waveform in this work, any waveform such as WCDMA (Wideband Code Division Multiple Access), LTE (Long Term Evolution), etc could also be implemented in a similar manner. As the standardization of function blocks of reconfigurable MD is finalized and deployed widely by ETSI RRS, a new market of RA codes will be emerging, which means the configuration of MD is determined very flexibly by downloading the desired RA codes from the Radio AppStore as described in this paper and [4]. It also implies that the modem functionality will be provided by the 3rd party, i.e., software modem provider, instead of MD or modem chip providers. This paper is to show the feasibility of such a flexible reconfigurable MD which is compliant with the standard being developed in ETSI RRS.

ACKNOWLEDGEMENTS

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